said PMOS transistor selectively providing power to said MOS transistor in response to said output signal of said controller circuit.

7. (Amended) A substrate bias generator according to claim 1, wherein said controller comprises:

an inverter which inverts said self refresh enable signal;

a NOR circuit having an input of said chip active enable signal and having input thereto [an inversion of] said inverted self refresh enable signal; and

an AND circuit having input thereto said output signal of said substrate voltage level detector and an output signal of said NOR circuit, said AND circuit controlling said first PMOS transistor.

REMARKS

Entry and consideration of the foregoing amendment and following remarks are respectfully requested under Rule 116. By this amendment, claims 1, 3-4 and 7 have been amended. Upon entry of this amendment, claims 1-5 and 7 will remain pending in the application.

Applicant appreciates Examiner's indication in the Advisory Action mailed July 15, 1996 that claim 2 is allowed.

In the Office Action mailed April 5, 1996, claims 1-5 and 7 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite.

Although the portions of claim 1 related to the "channel" noted by the Examiner in the rejection have been cancelled, similar language remains present in claim 4 and will, therefore, be addressed. It is notoriously well known that although enhancement MOS transistors have no channel formed when the device is constructed, a channel of charge carriers is formed when voltage is applied at the gate so that current results when voltage is applied across the drain-source terminals. This is called an "induced channel," and the devices are still classified as either "n-channel" or "p-channel" devices. Therefore, it is believed that the use of the term "channel" is appropriate, as further evidenced by the similar use of the term in U.S. Patent No. 5,329,168 to Sugibayashi, and that this rejection should be withdrawn.

The Examiner's suggested changes to claim 3 relating to the input of the chip enable signal have been proposed. Claims 3 and 7 have also been amended to further recite an inverter which inverts the self refresh enable signal to address the Examiner's concerns.

In view of the amendments to the claims and the foregoing remarks, the § 112 (second paragraph) rejection of the claims should be withdrawn.

Claims 1 and 4-5 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,329,168 to Sugibayashi et al. ("Sugibayashi"). Applicant respectfully traverses this rejection.

In accordance with an object of the present invention to provide a substrate bias generator which reduces current consumption during a self refresh mode, claim 1 (and similarly in claim 4) recites a controller which controls an operation of a substrate voltage level detector such that:

> said substrate voltage level detector is <u>not operative to drive said oscillator during a stand-by state of a self-refresh mode</u> of said semiconductor memory device.

By virtue of this patentable feature, current consumption by the substrate voltage level detector, and accordingly, the substrate bias generator, is markedly reduced during the self-refresh mode.

Sugibayashi does not suggest this feature. Sugibayashi merely teaches a substrate bias system which receives power either from an external power voltage or an internal power voltage. Nowhere does Sugibayashi contemplate the problem of current consumption during a stand-by state of a self refresh mode, much less the Applicant's solution whereby a substrate voltage level detector is rendered inoperative during this state.

For the foregoing reasons, amended independent claims 1 and 4 patentably define over the cited prior art.

Accordingly, the § 103 rejection of these claims, and claim 5 which depends from claim 4, should be withdrawn.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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